IN THE CLAIMS

Please **cancel** claim 1 without prejudice.

Please **amend** the claims as follows:

1. (Canceled)

2. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the at least one second-type diffusion region outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the second well comprises:

a first sub-well arranged between the insulating region and the first well and including the first second-type diffusion region; and

a second sub-well arranged between the insulating region and the third well and including the second second-type diffusion region,

wherein the insulating region is a third sub-well having the ~~a~~ first-type diffusion region.

3. (Currently amended) The semiconductor device of claim 2, wherein the first and second sub-wells of the second well are P-wells, and ~~the first voltage is applied to~~ the second-type diffusion regions of the first and second sub-wells of the second well are each connected to the first voltage terminal.

4. (Currently amended) The semiconductor device of claim 2, wherein the third sub-well is an N-well~~, and a second voltage is applied to the first-type diffusion region of the third sub-well~~.

5. (Original) The semiconductor device of claim 4, wherein ~~the first~~ a voltage applied to the first voltage terminal is a ground voltage, and the control ~~second~~ voltage generates a backward voltage between a base and an emitter of a bipolar junction transistor, the bipolar junction transistor comprising the first-type diffusion region of the first well, the second-type diffusion region of the first sub-well, and the first-type diffusion region of the third sub-well.

6. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the first and third wells are N-wells.

7. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the well bias voltage applied to the first-type diffusion region of the first well is a power supply voltage.

8. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein a region to which the pad is connected is a second-type diffusion region.

9. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities.

10. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the insulating region of the second well has a structure that surrounds the first well.

11. (Currently amended) The semiconductor device of claim 25 ~~1~~, wherein the third well constitutes a depletion-type MOS transistor.

12. (Currently amended) A semiconductor device comprising:

a first N-well connected to a pad to which an external pin is connected, the first N-well including an N-type diffusion region connected to ~~that receives~~ a ~~well~~ bias voltage terminal, and a P-type diffusion region formed in the vicinity of the pad;

a first P-well adjacent to the first N-well, the first P-well including an insulating region and at least one P-type diffusion region ~~that receives a ground voltage~~ outside the insulating region, the at least one P-type diffusion region of the first P-well outside of the insulating region is connected to a first voltage terminal; and

a second N-well adjacent to the first P-well and including an N-type diffusion region connected to the first voltage terminal ~~that receives the ground voltage~~,

wherein the insulating region is a sub-N-well embedded within said first P-well and having an N-type diffusion region connected to a second voltage terminal for receiving ~~that receives~~ an off mode control voltage for preventing a latch-up current.

13. (original) The semiconductor device of claim 12, wherein the at least one P-type diffusion region comprises a first P-type diffusion region and a second P-type diffusion region and the first P-well comprises:

a first sub-P-well located between the insulating region and the first N-well and including the first P-type diffusion region; and

a second sub-P-well located between the insulating region and the second N-well and including the second P-type diffusion region.

14. (original) The semiconductor device of claim 13, wherein the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region constitute a bipolar junction transistor which cuts off a current flowing from the first N-well to the second N-well.

15. (Currently amended) The semiconductor device of claim 14, wherein the control voltage provided to the second voltage terminal generates a backward voltage between a base and an emitter of the bipolar junction transistor composed of the N-type diffusion region of the first N-well, the P-type diffusion region of the first sub-P-well, and the N-type diffusion region of the insulating region.

16. (Currently amended) The semiconductor device of claim 12, wherein the ~~well~~bias voltage terminal connected ~~applied~~ to the N-type diffusion region of

the first N-well is adapted to receive a power supply voltage for the semiconductor device.

17. (Original) The semiconductor device of claim 12, wherein the insulating region of the first P-well has a structure that surrounds the first N-well.

18. (Original) The semiconductor device of claim 12, wherein the second N-well constitutes a depletion-type MOS transistor.

19. (Currently amended) A method of forming a semiconductor device comprising:

forming a first well connected to a pad to which an external pin is connected, the first well including a first-type diffusion region connected to ~~that receives a well~~ bias voltage terminal;

forming a second well adjacent to the first well, the second well including an insulating region having a first-type diffusion region and at least one second-type diffusion region outside the insulating region, wherein the at least one second-type diffusion region of the second well is connected to a first voltage terminal, and the first-type diffusion region of the insulating region is connected to a second voltage terminal; and

forming a third well adjacent to the second well and including a first-type diffusion region connected to the ~~that receives a~~ first voltage terminal,

wherein the insulating region inside the second well ~~having a first-type diffusion region~~, the at least one second-type diffusion region of the second well outside of the insulating region and ~~along with~~ the first-type diffusion region of the first well constitute a bipolar junction transistor which operates in a cut-off mode ~~and cuts~~ to cut off current flowing from the first well to the third well when a control voltage is applied to the second voltage terminal.

20. (Currently amended) The method of claim 19, wherein the at least one second-type diffusion region outside the insulating region comprises a first second-type diffusion region and a second second-type diffusion region, and the step of forming a second well comprises:

forming a first sub-well between the insulating region and the first well, the first sub-well including the first second-type diffusion region; and

forming a second sub-well between the insulating region and the third well, the second sub-well including the second second-type diffusion region,

wherein the insulating region is a third sub-well having the ~~a~~ first-type diffusion region.

21. (Currently amended) The method of claim 20, wherein the first and second sub-wells of the second well are P-wells, and ~~the first voltage is applied to~~ the second-type diffusion regions of the first and second sub-wells of the second well are each connected to the first voltage terminal.

22. (Currently amended) The method of claim 20, wherein the third sub-well is an N-well, ~~and a second voltage is applied to the first-type diffusion region of the third sub-well~~.

23. (Original) The method of claim 19, wherein the first and third wells are N-wells.

24. (Original) The method of claim 19, wherein the first-type diffusion regions are formed of N-type impurities, and the at least one second-type diffusion region is formed of P-type impurities.

25. (Currently amended) A semiconductor device comprising:

a first well connected to a pad to which an external pin is connected, the first well including a first-type diffusion region connected to a ~~first~~ bias voltage terminal;

a second well adjacent to the first well, the second well including an insulating region having a first-type diffusion region and at least one second-type diffusion region outside the insulating region, wherein the at least one second- type diffusion region of the second well is connected to a first ~~second bias~~ voltage terminal, and wherein the first-type diffusion region of the insulating region is connected to a ~~third bias~~ second voltage terminal; and

a third well adjacent to the second well and including a first-type diffusion region connected to the first ~~second bias~~ voltage terminal,

wherein the insulating region inside the second well, the at least one second-type diffusion region of the second well, and the first-type diffusion region of the first well, constitute a bipolar junction transistor which operates in a cut-off mode to cut off current from flowing from the first well to the third well when a control voltage is applied to the ~~third bias~~ second voltage terminal.